AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A semiconductor chip with a rectangular main surface and a functional element comprising:

a first side composing said main surface;

a second side ~~opposed~~ composing said main surface, wherein the second side is opposite to said first side;

a main electrode pad group composed of a plurality of main electrode pads, ~~which~~ wherein said plurality of main electrode pads is arranged on said main surface along said first side;

a first electrode pad group composed of a plurality of first electrode pads, which is located between said first side and said main electrode pad group with a first distance, wherein said plurality of first electrode pads is arranged ~~between said first side and said main electrode pad group~~ on said main surface along said first side;

a second electrode pad group composed of a plurality of second electrode pads, which is located between said second side and said main electrode group with a second distance that is longer than said first distance, wherein said plurality of second electrode pads is arranged on said main surface along said second side;

a plurality of first ~~interconnection connecting said~~ interconnections, wherein each first interconnection is connected between one of the main electrode ~~pad with said~~ pads and one of the first electrode ~~pad~~ pads; and

a plurality of second ~~interconnection connecting said~~ interconnections, wherein each second interconnection is connected between one of the main electrode ~~pad with said~~ pads and one of the second electrode ~~pad~~ pads,

wherein a main electrode pad connecting to a first electrode pad and a main electrode pad connecting to a second electrode pad are arranged alternately.

2. (Currently amended) The semiconductor chip according to claim 1,

wherein said first ~~interconnection~~ interconnections and said second ~~interconnection~~ interconnections are provided on said main surface of said semiconductor chip.

3. (Currently amended) The semiconductor chip according to claim 1,

wherein said first ~~interconnection~~ interconnections and said second ~~interconnection~~ interconnections are provided within said semiconductor chip.

4. (Currently amended) The semiconductor chip according to claim 3,

wherein any one or both of said first ~~interconnection~~ interconnections and said second ~~interconnection has or~~ interconnections have a multi-layer wired structure.

5. (Withdrawn) A semiconductor chip with a rectangular main surface comprising:

a first side composing said main surface;

a second side opposed to said first side;

a main electrode pad group composed of a plurality of main electrode pads, which plurality of main electrode pads is arranged on said main surface along said first side;

a first electrode pad group composed of a plurality of first electrode pads, which plurality of first electrode pads is arranged between said first side and said main electrode pad group;

a second electrode pad group composed of a plurality of second electrode pads, which plurality of second electrode pads is arranged on said main surface along said second side;

a plurality of conversion type interconnection connecting said main electrode pad with said first electrode pad one-on-one, which plurality of conversion type interconnection is provided on said main surface not in parallel with said main electrode pad group and said first electrode pad group; and

a plurality of second interconnections connecting said main electrode pad with said second electrode pad one-on-one, said plurality of second interconnections is arranged on said first main surface.

6. (Withdrawn) A semiconductor chip with a rectangular main surface comprising:

a first side composing said main surface;

a second side opposed to said first side;

a main electrode pad group composed of a plurality of main electrode pads, which plurality of main electrode pads is arranged on said main surface along said first side and has an area that is sufficiently wide so that two bonding wires can be connected thereto, respectively;

a second electrode pad group composed of a plurality of second electrode pads, which plurality of second electrode pads is arranged on said main surface along said second side; and

a second interconnection connecting said main electrode pad with said second electrode pad one-on-one.

7. (Withdrawn) The semiconductor chip according to claim 6,

wherein said main electrode pad is formed in a rectangular shape and has a sufficiently wide area so that, two bonding wires can be connected thereto;

a longer direction of said rectangular shape is elongated in a direction orthogonal to said first side; and

said main electrode pad is separated into a first partial main electrode pad at said first side, to which one of said bonding wires is connected, and a second partial main electrode pad, to which the other one of said bonding wires is connected.

8. (Withdrawn) The semiconductor chip according to claim 7,

wherein said main electrode pad further includes a connection area connecting said first partial main electrode pad with said second partial main electrode pad so that a width in a direction orthogonal to the direction in which said main electrode pad is elongated is narrower than the widths of said first and second partial electrode pads.

9. (Withdrawn) The semiconductor chip according to claim 8,

wherein said second electrode pad is formed in a rectangular shape and has an area to which two bonding wires can be connected;

a longer direction of said rectangular shape is elongated in a direction orthogonal to said second side; and

said second electrode pad is separated into a first partial electrode pad at said second side, to which one of said bonding wires is connected, and a second partial electrode pad, which adjoins said first partial electrode pad and to which the other one of said bonding wires is connected.

10. (Withdrawn) The semiconductor chip according to claim 9,

wherein the number of said first electrode pads is less than the number of said main

electrode pads, and said first interconnection is connected to an electrode pad which is different from the electrode pad, to which said second interconnection is connected, from among said plurality of main electrode pads.

11. (Withdrawn) The semiconductor chip according to claim 10,

wherein, in said main electrode pad group, an electrode pad, to which said first interconnection is connected, and an electrode pad, to which said second interconnection is connected, are alternately arranged.

12. (Withdrawn) The semiconductor chip according to claim 9,

wherein an interconnection connecting said main electrode pads with said second electrode pads of the same number as said main electrode pads one by one is provided.

13. (Currently amended) The semiconductor chip according to claim 1,

wherein any one or both of said first and second ~~interconnection is or~~ interconnections are formed within ~~the~~ a same wired layer.

14. (Currently amended) The semiconductor chip according claim 1,

wherein said semiconductor chip is provided with a multi-layer wired structure; and

any one or both of said first and second interconnections has or have [[a]] the multi-layer wired structure, ~~to~~ which comprises a plurality of wired ~~layer is~~ layers connected through a via embedded in ~~which~~ a via hole ~~is embedded~~.

15. (Currently amended) The semiconductor chip according to claim 1,

wherein circuit elements having weak tolerance to the stress are integrated in the vicinity of ~~the~~ a lower side of said main electrode pad group.

16. (Currently amended) A semiconductor device comprising:

a substrate having a ~~main~~ first front surface having a first range on which a first bonding pad is formed, a second range on which a second bonding pad is formed, and a third range existing between said first range and said second range;

a first ~~plurality of~~ semiconductor ~~chips with the same configuration to be~~ chip having a rectangular main surface and a functional element laminated in said third range of said ~~main~~

first front surface ~~or to be further mounted in the other~~; said first semiconductor chip ~~laminated in said third range; each of said plural semiconductor chips with a rectangular main surface~~ having a first side composing said main surface; a second side ~~opposed~~ composing said main surface, wherein the second side is opposite to said first side; a main electrode pad group composed of a plurality of main electrode pads, ~~which~~ wherein said plurality of main electrode pads is arranged on said main surface along said first side; a first electrode pad group composed of a plurality of first electrode pads[[,]] which is located between said first side and said main electrode pad group with a first distance, wherein said plurality of first electrode pads is arranged on said main surface along ~~between~~ said first side ~~and said main electrode pad group~~, a second electrode pad group composed of a plurality of second electrode pads[[,]] which is located between said second side and said main electrode group with a second distance which is longer than said first distance, wherein plurality of second electrode pads is arranged on said main surface along said second side; a plurality of first ~~interconnection connecting said~~ interconnections, wherein each first interconnection is connected between one of the main electrode ~~pad with said~~ pads and one of the first electrode ~~pad~~ pads; and a plurality of second ~~interconnection connecting said~~ interconnections, wherein each second interconnection is connected between one of the main electrode ~~pad with said~~ pads and one of the second electrode ~~pad~~ pads;

a second semiconductor chip having the same configuration of the first semiconductor chip and mounted on said first semiconductor chip laminated in said main surface;

a first bonding wire electrically connecting between said first bonding pad ~~with~~ and said first electrode pad of said first semiconductor;

a second bonding wire electrically connecting between said main electrode pad of said first semiconductor chip ~~with~~ and a first electrode pad of ~~the other~~ said second semiconductor chip, wherein said main electrode pad of said first semiconductor chip is connected with said first electrode pad of said first semiconductor chip ~~to be mounted on~~ through said first interconnection of said first semiconductor chip;

a third bonding wire electrically connecting between said main electrode pad of said first semiconductor chip ~~with~~ and a main electrode pad of ~~the other~~ said second semiconductor chip ~~to be mounted on said semiconductor chip~~, wherein said main electrode pad of said first semiconductor chip is connected with said second electrode pad of said first semiconductor chip through said second interconnection of said first semiconductor chip, and said main electrode pad of said second semiconductor chip is connected with a second

electrode pad of said second semiconductor chip through a second interconnection of said second semiconductor chip; and

a fourth bonding wire electrically connecting between said second bonding ~~wire with~~ pad and said second electrode pad of said second semiconductor chip;

wherein, in said ~~plural~~ first semiconductor ~~chips~~ chip and said second semiconductor chip, said ~~each~~ first side ~~is~~ of said first semiconductor chip and a first side of said second semiconductor chip are located at the same side, ~~each~~ said main surface ~~is~~ of said first semiconductor ship and a main surface of said second semiconductor chip are turned in the same direction, and said main electrode pad and said first electrode pad of said first semiconductor chip are located at ~~the lower side are located at~~ the outside from ~~the~~ a first side of said ~~other~~ second semiconductor chip ~~located at the upper side and said plural semiconductor chips are laminated each other~~.

17. (Withdrawn) A semiconductor device comprising:

a substrate having a main surface having a first range on which a first bonding pad is formed, a second range on which a second bonding pad is formed, and a third range existing between said first range and said second range;

a plurality of semiconductor chips with the same configuration to be laminated in said third range of said main surface or to be further mounted in the other semiconductor chip laminated in said third range; each of said plural semiconductor chips with a rectangular main surface having a first side composing said main surface; a second side opposed to said first side; a main electrode pad group composed of a plurality of main electrode pads, which plurality of main electrode pads is arranged on said main surface along said first side; a first electrode pad group composed of a plurality of first electrode pads, which plurality of first electrode pads is arranged between said first side and said main electrode pad group; a second electrode pad group composed of a plurality of second electrode pads, which plurality of second electrode pads is arranged on said main surface along said second side; a plurality of conversion type interconnections electrically connecting said main electrode pad with said first electrode pad one-on-one, said plurality of conversion type interconnection is provided on said main surface not in parallel with said main electrode pad group and said first electrode pad group; and

a plurality of second interconnections electrically connecting said main electrode pad with said second electrode pad one-on-one;

a first bonding wire electrically connecting said first bonding pad with said first electrode pad;

a second bonding wire electrically connecting said main electrode pad of said semiconductor chip with a main electrode pad of the other semiconductor chip to be mounted on said semiconductor chip; and

a third bonding wire electrically connecting said second bonding wire with a second electrode pad of said other semiconductor chip;

wherein, in said plural semiconductor chips, said each first side is located at the same side, each main surface is turned in the same direction, and said main electrode pad and said first electrode pad of said semiconductor chip located at the lower side are located at the outside from the first side of said other semiconductor chip located at the upper side and said plural semiconductor chips are laminated each other.

18. (Withdrawn) A semiconductor device comprising:

a substrate having a main surface having a first range on which a first bonding pad is formed, a second range on which a second bonding pad is formed, and a third range existing between said first range and said second range;

a plurality of semiconductor chips with the same configuration to be laminated in said third range of said main surface or to be further mounted in the other semiconductor chip laminated in said third range; each of said plural semiconductor chips with a rectangular main surface wherein a longer direction of said rectangular shape is elongated in a direction orthogonal to said first side; having a first side composing said main surface; a second side opposed to said first side; an area sufficiently wide so that two bonding wires arranged on said main surface along said first side can be connected thereto; a main electrode pad group composed of a plurality of main electrode pads, which plurality of main electrode pads is separated into a first partial electrode pad at said first side and a second partial electrode pad; a second electrode pad group composed of a plurality of second electrode pads, which plurality of second electrode pads is arranged on said main surface along said second side; and a plurality of second interconnections electrically connecting said main electrode pad with said second electrode pad one-on-one;

a first bonding wire electrically connecting said first bonding pad with said first partial main electrode pad;

a second bonding wire electrically connecting said second partial main electrode pad

of said semiconductor chip with a first partial main electrode pad of the other semiconductor chip to be mounted on said third range of said semiconductor chip;

a third bonding wire electrically connecting said second partial main electrode pad of said semiconductor chip with a second partial main electrode pad of the other semiconductor chip to be mounted on said third range of said semiconductor chip; and

a fourth bonding wire electrically connecting said second bonding pad with a second electrode pad of said other semiconductor chip;

wherein, in said plural semiconductor chips, said each first side is located at the same side, each main surface is turned in the same direction, and said main electrode pad and said first electrode pad of said semiconductor chip located at the lower side are located at the outside from the first side of said other semiconductor chip located at the upper side and said plural semiconductor chips are laminated each other.

19. (Withdrawn) The semiconductor device according to claim 18,

wherein said main electrode pad of said semiconductor chip further includes a connection area connecting said first partial main electrode pad with said second partial main electrode pad so that a width in a direction orthogonal to the direction in which said main electrode pad is elongated is narrower than the widths of said first and second partial electrode pads.

20. (Withdrawn) A semiconductor device comprising:

a substrate having a main surface having a first range on which a first bonding pad is formed, a second range on which a second bonding pad is formed, and a third range existing between said first range and said second range;

a first semiconductor chip to be laminated in said third range of said main surface; said first semiconductor chip with a rectangular main surface wherein a longer direction of said rectangular shape is elongated in a direction orthogonal to said first side; having a first side composing said main surface; a second side opposed to said first side; an area sufficiently wide so that two bonding wires arranged on said main surface along said first side can be connected thereto; a main electrode pad group composed of a plurality of main electrode pads, which plurality of main electrode pads is separated into a first partial main electrode pad at said first side and a second partial main electrode pad; a second electrode pad group composed of a plurality of second electrode pads, which plurality of second electrode

pads is arranged on said main surface along said second side; and a plurality of second interconnections electrically connecting said main electrode pad with said second electrode pad one-on-one;

a second semiconductor chip having the same configuration as that of said first semiconductor chip, which is mounted on said first semiconductor chip;

a third semiconductor chip having the same configuration as those of said first and second semiconductor chips, which are mounted on said second semiconductor chip;

a first bonding wire connecting said first partial main electrode pad of said first semiconductor chip with said first bonding pad of said substrate;

a second bonding wire connecting said second partial main electrode pad of said first semiconductor chip with a first partial main electrode pad of said second semiconductor chip;

a third bonding wire connecting said second partial main electrode pad of said second semiconductor chip with a first partial main electrode pad of said third semiconductor chip; and

a fourth bonding wire connecting said second electrode pad of said third semiconductor chip with said second bonding pad of said substrate;

wherein, in said plural semiconductor chips, said each first side is located at the same side, each main surface is turned in the same direction, and said main electrode pad and said first electrode pad of said semiconductor chip located at the lower side are located at the outside from the first side of said other semiconductor chip located at the upper side and said plural semiconductor chips are laminated each other.

21. (Withdrawn) The semiconductor device according to claim 20,

wherein said second electrode pad further includes a connection area connecting said first partial electrode pad with said second partial electrode pad so that a width in a direction orthogonal to the direction in which said main electrode pad is elongated is narrower than the widths of said first and second partial electrode pads.

22. (Withdrawn) A semiconductor device comprising:

a substrate having a main surface having a first range on which a first bonding pad is formed, a second range on which a second bonding pad is formed, and a third range existing between said first range and said second range;

a first semiconductor chip to be laminated in said third range of said main surface;

said first semiconductor chip with a rectangular main surface wherein a longer direction of said rectangular shape is elongated in a direction orthogonal to said first side; having a first side composing said main surface; a second side opposed to said first side; an area sufficiently wide so that two bonding wires arranged on said main surface along said first side can be connected thereto; a main electrode pad group composed of a plurality of main electrode pads, which plurality of main electrode pads is separated into a first partial main electrode pad at said first side and a second partial main electrode pad; wherein a longer direction of said rectangular shape is elongated in a direction orthogonal to said second side; having an area sufficiently wide so that two bonding wires arranged on said main surface along said second side can be connected thereto; a second electrode pad group composed of a plurality of second electrode pads, which plurality of second electrode pads is separated into a first partial electrode pad at said second side and a second partial electrode pad; and a plurality of second interconnections connecting said main electrode pad with said second electrode pad one-on-one;

a second semiconductor chip having the same configuration as that of said first semiconductor chip, which is mounted on said third semiconductor chip;

a third semiconductor chip having the same configuration as those of said first and second semiconductor chips, which is mounted on said first semiconductor chip;

a fourth semiconductor chip having the same configurations as those of said first, second, and third semiconductor chips, which is mounted on said second semiconductor chip;

a fifth semiconductor chip having the same configurations as those of said first, second, third and fourth semiconductor chips, which is mounted across said third and fourth semiconductor chips;

a first bonding wire connecting said first partial main electrode pad of said first semiconductor chip with said first bonding pad of said substrate;

a second bonding wire connecting said second partial main electrode pad of said first semiconductor chip with a first partial main electrode pad of said third semiconductor chip;

a third bonding wire connecting said second partial main electrode pad of said third semiconductor chip with a first partial main electrode pad of said fifth semiconductor chip;

a fourth bonding wire connecting said first partial electrode pad of said fifth semiconductor chip with said second partial electrode pad of said fourth semiconductor chip;

a fifth bonding wire connecting said first partial electrode pad of said fourth semiconductor chip with said second partial electrode pad of said second semiconductor chip;

and

a sixth bonding wire connecting said first partial electrode pad of said second semiconductor chip with said second bonding pad of said substrate;

wherein said first and second semiconductor chips are laminated in said third range with said each first side located serially at the same side, each main surface is turned in the same direction; said third and fourth semiconductor chips are laminated with said main electrode pad and said first electrode pad of said first and second semiconductor chips located at the lower side are located at the outside from the first side of said other semiconductor chip located at the upper side; and said fifth chip is laminated with said main electrode and said first electrode pad of said third chip and said second electrode pad of said fourth semiconductor chip exposed.

23. (Withdrawn) The semiconductor device according to claim 22,

wherein said main electrode pad further includes a connection area connecting said first partial main electrode pad with said second partial main electrode pad so that a width in a direction orthogonal to the direction in which said main electrode pad is elongated is narrower than the widths of said first and second partial electrode pads.

24. (Withdrawn) The semiconductor device according to claim 23,

wherein said second electrode pad further includes a connection area connecting said first partial main electrode pad with said second partial main electrode pad so that a width in a direction orthogonal to the direction in which said second electrode pad is elongated is narrower than the widths of said first and second partial electrode pads.

25. (Withdrawn) The semiconductor chip according to claim 22,

wherein an interconnection connecting said main electrode pads with said second electrode pads of the same number as said main electrode pads one by one is provided.

26. (Currently amended) The semiconductor chip according to claim 16,

wherein circuit elements having weak tolerance to the stress are integrated in the vicinity of ~~the~~ a lower side of said main electrode pad group.

27. (Currently amended) The semiconductor chip according to claim 16,

wherein said substrate is provided with a via hole passing through from said first front surface to ~~said~~ a second surface of the substrate, a via embedded in the via hole and connected to one of said plurality of first and second bonding pads ~~having said via hole embedded therein~~, and an external terminal connected to said via; and said substrate is further provided with a sealing portion sealing all bonding wires on said substrate.